**--Full Adder – Behavioral Model**

**1. Code**

**----------------------------------------------------------------------------------**

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

use IEEE.STD\_LOGIC\_ARITH.ALL;

use IEEE.STD\_LOGIC\_UNSIGNED.ALL;

entity FULL\_ADDER1 is

Port ( a,b,c : in STD\_LOGIC;

s,cr : out STD\_LOGIC);

end FULL\_ADDER1;

architecture Behavioral of FULL\_ADDER1 is

begin

process (a,b,c)

begin

if (a='0' and b='0' and c='0' ) then

s <= '0';

cr <= '0';

elsif (a='0' and b='0' and c='1' ) then

s <= '1';

cr <= '0';

elsif (a='0' and b='1' and c='0' ) then

s <= '1';

cr <= '0';

elsif (a='0' and b='1' and c='1' ) then

s <= '0';

cr <= '1';

elsif (a='1' and b='0' and c='0' ) then

s <= '1';

cr <= '0';

elsif (a='1' and b='0' and c='1' ) then

s <= '0';

cr <= '1';

elsif (a='1' and b='1' and c='0' ) then

s <= '0';

cr <= '1';

else

s <='1';

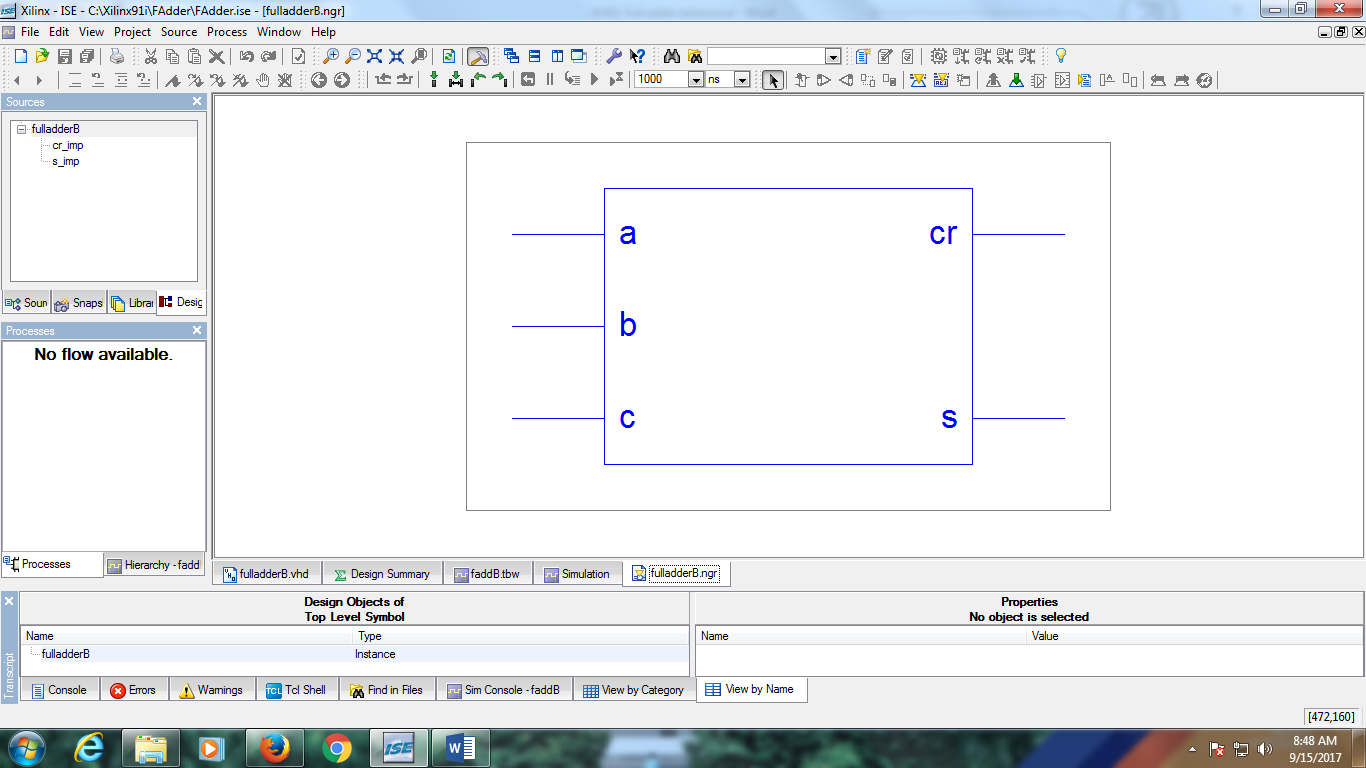
cr <='1';

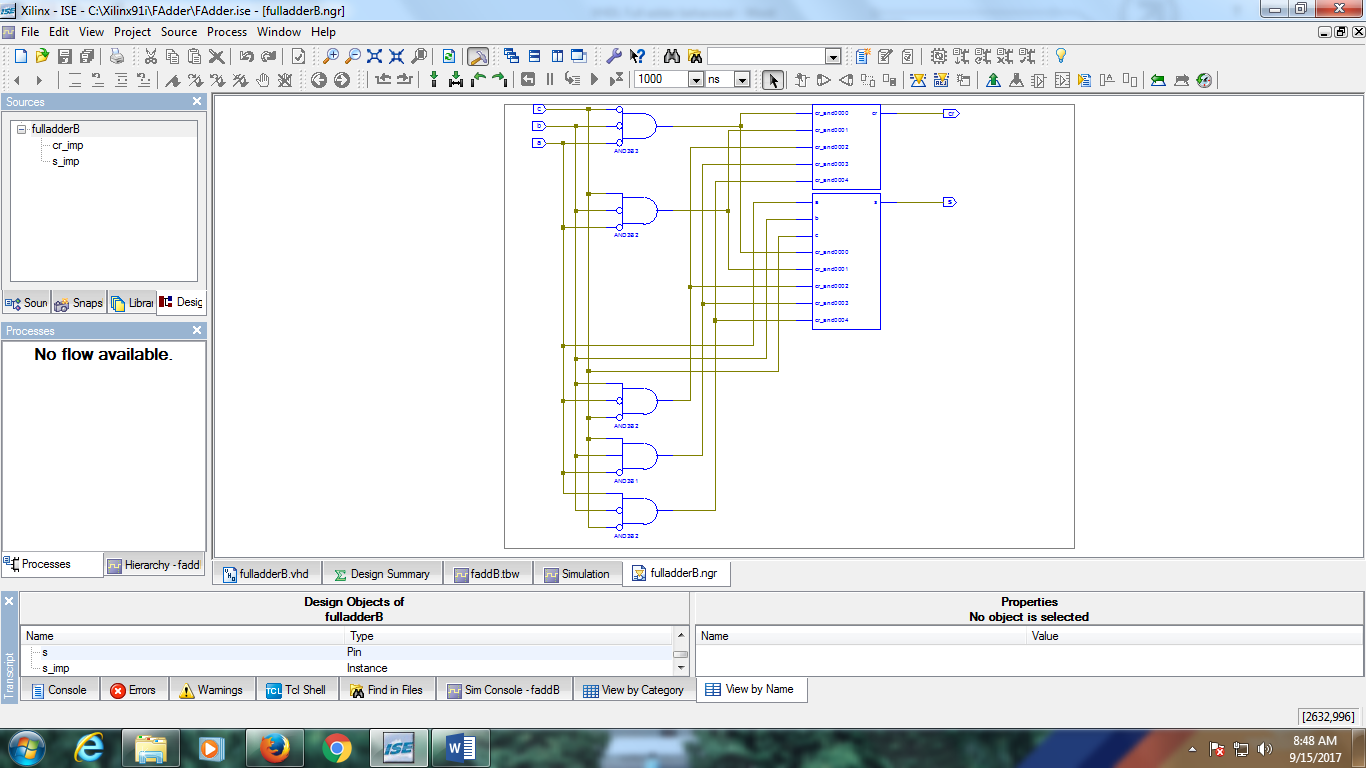
end if ;

end process ;

end Behavioral;

**2. RTL schematic**





**3. Simulation Output**

